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FOR

ON-DRAM TERMINATION RESISTANCE CONTROL CIRCUIT AND METHOD THEREOF

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ON-DRAM TERMINATION RESISTANCE CONTROL CIRCUIT AND METHOD THEREOF

Field of the Invention

The present invention relates to a resistance control circuit for an IC (Integrated Circuit) termination; and, more particularly, to a resistance control circuit for controlling resistance of an IC termination based on an externally coupled resistor.

Background of the Invention

Generally, a resistor of an IC termination is needed to make signal transmission between devices smooth. When resistances are not matched properly, the transmitted signal may be reflected to cause errors in signal transmission. However, if a fixed resistor is given externally for this matching, resistances cannot be matched properly due to decline of the IC, temperature change, or difference of manufacturing process. For this, a new technique is introduced for controlling the resistance of the IC termination by controlling the number of turned-on transistors among transistors, which are coupled in parallel, to have same resistance as an external reference resistor.

U.S. Patent No. 6,087,847 issued on July 11, 2000 discloses an IC including a digital feedback control circuit

for controlling an impedance of an interface circuit output buffer based on impedance control of non-data signal output buffer that is partially coupled to an external impedance, to suggest a circuit for varying a resistance at an output buffer such as a micro-processor. However, a non-data signal output buffer as shown in Fig. 2 in U.S. Patent No. 6,087,847 uses an output buffer having same type as an interface circuit output buffer, which has so many logic devices used for impedance control. Therefore, the area for the circuit for controlling the impedance within the IC is to be increased. Further, because U.S. Patent No. 6,087,847 connects only one of a power voltage and a ground voltage for the output buffer, it cannot be used for resistance control of the termination that is operated by simultaneously turning on switches that is connected to both of the power voltage and the ground voltage.

Summary of the Invention

It is, therefore, an objective of the present invention to provide a resistance control circuit of an IC termination capable of controlling the resistance of the IC termination and minimizing the area for the resistance control circuit by using a simplified circuit scheme.

In accordance with an aspect of the present invention, there is provided an on-DRAM termination resistance control circuit for adjusting a resistance within a semiconductor memory device that performs an on-DRAM termination operation,

including a push-up resistance adjusting unit for adjusting resistances of a first and a second inner resistors based on an external reference resistor; a pull-down resistance adjusting unit for adjusting a resistance of a third resistor based on the second inner resistor that is adjusted by the push-up resistance control unit; and a resistance adjustment control unit for controlling to alternatively repeat the operation of the push-up resistance adjusting unit and the pull-down resistance adjusting unit for a predetermined number of adjustment times.

Desirably, the push-up resistance adjusting unit of the present invention includes a comparing unit for comparing a voltage between both ends of the external reference resistor that is coupled to the first inner resistor with a reference voltage; and a resistance adjusting unit for adjusting the resistances of the first and the second inner resistors depending on the output of the comparing means, and the first and the second inner resistors vary their resistances depending on the output of the resistance adjusting unit.

Desirably, the resistance adjusting unit of the present invention includes a calculating unit for up-counting a signal having predetermined bits by one when receiving the output of the comparing unit; and a first and second push-up decoding unit for adjusting the first and the second inner resistors by decoding the output of the calculating unit, respectively.

Desirably, the pull-down resistance adjusting unit of the present invention includes a comparing unit for comparing

the voltage between both ends of the third inner resistor that is coupled to the second inner resistor with a reference voltage; and a resistance adjusting unit for adjusting the resistance of the third inner resistor depending on the output of the comparing unit, and the third inner resistor varies its resistance depending on the output of the resistance adjusting unit.

Desirably, the resistance adjusting unit includes a calculating unit for up-counting a signal of predetermined bits by one when receiving the output of the comparing unit; and a pull-down decoding unit for decoding the output of the calculating unit to adjust the resistance of the third inner resistor.

Desirably, the resistance adjustment controlling unit of the present invention includes a ring oscillator controlling unit for outputting a control signal to start an operation and finish the operation for the predetermined number of times depending on a resistance adjust command from external; a ring oscillator for outputting a pulse at every cycle while oscillating based on the control signal that is outputted from the ring oscillator controlling unit; and a pulse counting and comparing unit for counting the pulses from the ring oscillator and comparing the number of the counted pulses with the predetermined number of times to confirm equality of both numbers.

Desirably, the ring oscillator controlling unit of the present invention includes a first PMOS transistor receiving a

power-up signal as its control signal, one end of the first PMOS transistor being coupled to a power voltage; a first NMOS transistor receiving an enable input signal as its control signal, coupled to the other end of the first PMOS transistor and a ground voltage; a first inverter receiving the output of the pulse counting and comparing means as its input; a second PMOS transistor receiving the output of the first inverter as its control signal, coupled to the power voltage and the other end of the first PMOS transistor; a oppositely parallel coupled pair of a second and a third inverters coupled the other end of the first PMOS transistor; and fourth and a fifth inverters, serially coupled to each other, receiving the output of the second inverter as its input.

Desirably, the ring oscillator of the present invention includes a NOR gate receiving the output of the fourth inverter at one of its two inputs; a sixth and a seventh inverters, serially coupled to each other, for buffering the output of the NOR gate; en eighth and a ninth inverters, serially coupled to each other, for buffering the output of the seventh inverter to output to the other input of the NOR gate; and a tenth, an eleventh and a twelfth inverters for buffering and inverting the output of the ninth inverter.

Desirably, the pulse counting and comparing unit of the present invention includes a pulse counter for counting the pulses outputted from the twelfth inverter; and an adjustment times comparing means for comparing the output of the pulse counter with the predetermined number of adjustment.

Also, an on-DRAM termination resistance control method for adjusting a resistance within a semiconductor memory device that performs an on-DRAM termination operation, includes the steps of (a) adjusting resistances of a first and a second inner resistors based on an external reference resistor; (b) adjusting a resistance of a third resistor based on the second inner resistor that is adjusted at the step (a); and (c) alternatively repeating the steps (a) and (b) for a predetermined number of adjustment times.

Desirably, the step (a) of the present invention includes the steps of (d) comparing the voltage between both ends of the external reference resistor coupled to the first inner resistor; and (e) adjusting the resistances of the first and the second inner resistors depending on the comparison result of the step (d).

Desirably, the step (b) of the present invention includes the steps of (f) comparing the voltage between both nds of the third inner resistor coupled with the second inner resistor; and (g) adjusting the resistance of the third inner resistor depending on the comparison result of the step (f).

Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

Fig. 1 provides an overall block diagram including an ODT resistance control circuit in accordance with the present invention;

Fig. 2 is a block diagram of an embodiment of an ODT resistance adjustment control circuit in accordance with the present invention;

Fig. 3 describes an embodiment of a ring oscillator control unit in accordance with the present invention;

Fig. 4 shows an embodiment of a ring oscillator unit in accordance with the present invention;

Fig. 5 presents an embodiment of a pulse counting and comparing circuit in accordance with the present invention; and

Fig. 6 illustrates a timing diagram of an ODT resistance control circuit in accordance with an embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Hereinafter, with reference to the accompanying drawings, a preferred embodiment of the present invention will be explained in detail.

Fig. 1 provides an overall block diagram including an ODT (on-DRAM termination) resistance control circuit in accordance with the present invention.

The ODT resistance control circuit 110 according to the present invention is constructed to respectively provide a PU

(push-up) code and a PD (push-down) code to a push-up decoder and a pull-down decoder of an interface circuit 120 that is performs the on-DRAM termination operation.

It will be described in detail for the operation of the ODT resistance control circuit 110 according to an embodiment of the present invention. It may be designed such that 4 of 8 parallel coupled transistors 201, 210, 211 (only 4 shown in Fig. 1) for forming an inner resistor are to be turned on when the ODT resistance control circuit 110 is enabled. At this point, when a first inner resistor 201 varies compared with an external reference resistor Rref, the voltage between both ends of the external reference resistor Rref (i.e., a voltage on a node A) varies in turn. After that, a first comparator 203 compares a reference voltage Vref being half of a power voltage with the voltage on the node A to output a logic signal having one of "H" state and "L" state.

When the outputted logic signal is inputted to a first calculating unit 205, the first calculating unit 205 provides a first push-up decoder 207 and a second push-up decoder 209 with "101" or "011" that is changed from "100" depending on the inputted logic signal. The first push-up decoder 207 and the second push-up decoder 209 adjust the resistances of the first inner resistor 201 and the second inner resistor 210 depending on the input signals. When a voltage on a node B changes depending on the adjusted inner resistor 210, a second comparator 213 receiving the voltage on the node B and the reference voltage Vref as its inputs outputs a logic signal

having one of "H" state and "L" state.

When the outputted logic signal is inputted to the second calculating unit 215, the second calculating unit 215 outputs "101" or "011" changed from initial "100" depending on the inputted logic signal so that a pull-down decoder 217 adjust the resistance of the inner resistor 211.

As above, the operation of the push-up resistance adjusting units 201, 203, 205, 207, 209, 210 and the pull-down resistance adjusting units 211, 213, 215, 217 will be stopped by a control signal that is outputted from an ODT resistance adjustment control unit 219 or finished when the resistance of the inner resistor becomes equal to that of the external reference resistor.

That is, an on-DRAM termination resistance control method for adjusting a resistance within a semiconductor memory device that performs an on-DRAM termination operation in accordance with the present invention comprises the steps of (a) adjusting resistances of a first and a second inner resistors based on an external reference resistor, (b) adjusting a resistance of a third resistor based on the second inner resistor that is adjusted at the step (a), and (c) alternatively repeating the steps (a) and (b) for a predetermined number of adjustment times.

Particularly, the step (a) of the present invention includes the steps of (d) comparing the voltage between both ends of the external reference resistor coupled to the first inner resistor with a reference voltage, and (e) adjusting the

resistances of the first and the second inner resistors depending on the comparison result of the step (d).

Further, the step (b) of the present invention includes the steps of (f) comparing the voltage between both ends of the third inner resistor coupled to the second inner resistor with a reference voltage, and (g) adjusting the resistance of the third inner resistor depending on the comparison result of the step (f).

Fig. 2 is a block diagram of an embodiment an ODT resistance control circuit in accordance with the present invention.

The ODT resistance adjustment control circuit 219 includes a ring oscillator controlling unit 310, a ring oscillator unit 320 and a pulse counting and comparing unit 330. The ring oscillator controlling unit 310 provides the ring oscillator unit 320 with a signal for operating depending on a resistance adjustment command from external. The ring oscillator unit 320 oscillates to output pulses CP1, CP2. The pulse counting and comparing unit 330 counts the number of the pulses CP1 inputted from the ring oscillator unit 320, i.e., the number of times of actual resistance adjustment operations and then compare it with the number of commanded adjustment times to provide comparison result to the ring oscillator controlling unit 310. The ring oscillator controlling unit 310 determines whether to continue the operation or to finish depending on the comparison result. That is, when the number of times of actual resistance adjustment operations reaches

the number of commanded adjustment times, the ring oscillator controlling unit 310 provides a signal for stopping the operation to the ring oscillator unit 320 so that the ring oscillator unit 320 finishes its operation.

Fig. 3 describes an embodiment of a ring oscillator control unit in accordance with the present invention, Fig. 4 shows an embodiment of a ring oscillator unit in accordance with the present invention, and Fig. 5 presents an embodiment of a pulse counting and comparing unit in accordance with the present invention.

It will be described for signals that are inputted to Fig. 3. A signal Y/N keeps its state in Y ("H" state) if the number of times of actual adjustment operations is equal to the number of commanded adjustment times and, if else, it keeps its state in N ("L" state). A power-up signal pwrup keeps its state in "H" when power is turned on. An enable input signal enable_in keeps its state in "H" when the operation of the ODT resistance adjustment controlling unit 219 is enabled.

Using the above signals as its inputs, when the enable input signal enable_in of the ring oscillator controlling unit in Fig. 3 transits to "H" state, there are subsequent transits to "L" state on a node C, to "L" state on a node D, and to "H" state on a node E. Finally, An enable output bar signal enable_outb outputs "L" state.

When the enable output bar signal enable_outb of "L" state is inputted to a NOR gate 321 in Fig. 4, an F node and

the pulse CP2 transit to "H" state and the pulse CP1 outputs "L" state with a delay from the pulse CP2 by a predetermined delay time.

After performing such an operation for the predetermined commanded adjustment times, when the signal Y/N from the pulse counting and comparing unit 330 transits to "H", a PMOS transistor 314 is turned on to make an H node have "H" state. Accordingly, the enable output bar enable_outb transits to "H" state. When the enable output bar signal enable_outb of "H" state is inputted to the NOR gate 321, the F node and the pulse CP2 transit to "L" state and the pulse CP1 outputs "H" state with a delay from the pulse CP2 by predetermined delay time.

Briefly describing for Fig. 5, a pulse counter 331 counts the pulses CP1 inputted from the ring oscillator unit 320. An adjustment times comparing unit 332 compares the number of the actual adjustment times with the number of the commanded adjustment times to output a signal having "H" when two numbers are equal to each other. At this time, the pulse counter 331 uses the signal of "H" state when two numbers are equal to each other as a reset signal to reset the pulse counter 331.

Fig. 6 illustrates a timing diagram of an ODT resistance control circuit in accordance with an embodiment of the present invention.

In an embodiment, there are provided 4 operations that are performed by using rising edge triggering and falling edge

triggering of the pulses CP1, CP2.

As described above, according to the present invention, the IC termination resistance control circuit and the method thereof can adjust the termination resistance in the IC and minimize the area of the circuit with the simplified circuit scheme.

Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.